Skipper™

Integrated Chip-Finishing Layout Platform

Highlights

- One of the fastest tools for importing and viewing layout data
- Unique “layout server” mode to share layout data
- Large data handling capacity—over 100GB GDS
- Integrated chip-finishing platform
  - Layout editing, net tracing, P2P resistance analysis and Boolean operations
  - Comprehensive search mechanisms
  - Fastest layout comparison
  - DRC/LVS debugging
  - Cell swapping and IP merging
- Focused ion beam (FIB) data processing
- 3D viewing for layout inspection
- Layout watermark and log information
- TCL script supported

Introduction

Architected with an optimized database, highly effective memory management system and unified GUI, Skipper is an easy-to-use chip-finishing platform and capable of handling large layouts (over 100GB GDS).

Built-in applications include:

- Merging standard cells and IPs
- Layout editing, hierarchically delete, net tracing, searching, and Boolean operations
- Handling fast layout vs. layout comparison in GUI and batch mode.
- Seal-ring sizing
- Debugging DRC/LVS results
- Preparing FIB data for device analysis and instruction for FIB operation.

Skipper enhances designer productivity and accelerates tape-out.

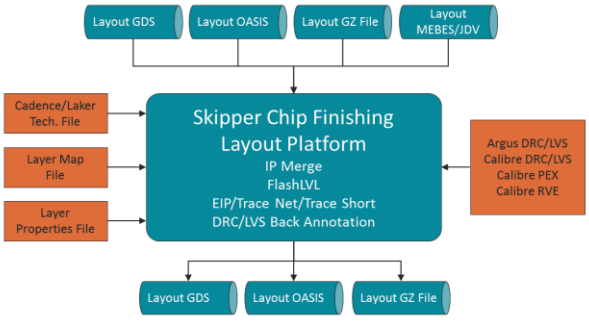

Fig1. Skipper Layout Platform

Fast Importing and Viewing of Layout

Skipper’s built-in layout engine is designed to read and process GDS data extremely fast. Skipper’s performance is illustrated in Fig 2, across many layouts. Layout server mode improves loading speed further.

Cases	File Size (gz/unzip)	Layers	Loading Time	Speed
1	16G /138G	213	962 Sec	60
2	756M/4.3G	195	36 Sec	141
3	1.04G/8.2G	150	53 Sec	199
4	5.76G/50G	210	506 Sec	353

Fig2. Benchmark Results

Large Data-Handling Capacity

Skipper can handles GDSII layouts greater than 100 GB in size. Together with its multi-threading echnology, Skipper offers the best capacity and scalability users need.

Integrated Chip-Finishing Platform

Built in functions that enable faster and better chip finishing including layout editing, net tracing, searching, Boolean operations and sizing of seal-ring. Hierarchical search based on “instance”, “label”, and “shape” is supported along with result highlighting and zooming. AND/OR/NOT/XOR operations can be performed on layers or shapes.

The ***trace net*** function allows a large net such as VDD/VSS, containing thousands of polygons, to be traced and highlighted in minutes. Traced by name is also supported.

The ***trace short*** function helps users find the connected path between two shapes. And traced results can be saved to a GDSII file.

Fig3. Net Connectivity Tracing

P2P Resistance Analysis: Skipper supports point to point resistance extraction and current density calculation, the effective R value between any 2 points in a certain net can be output based on itf file, the current density of each part of the net can be generated and highlighted in the layout.

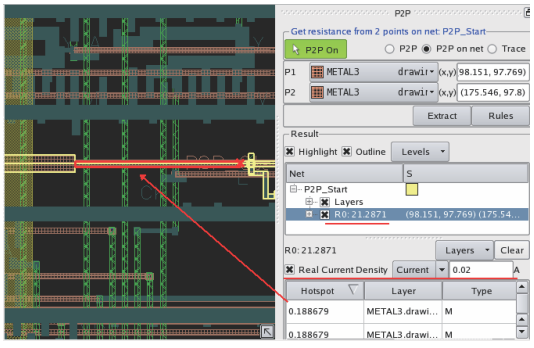

Fig4. P2P Resistance Analysis

DRC/LVS Debug: Skipper supports full-chip level DRC/LVS debugging including setting waivers, eliminating duplicate errors and generating DRC reports. Argus™ and third party DRC/LVS tool are supported.

Cell Swap and IP Merge: Skipper provides merging in standard cells and IP blocks to replace footprints, switch cells and add seal rings, dummy cells can be inserted in the same process. Layouts from multiple databases can be merged using either script or GUI modes.

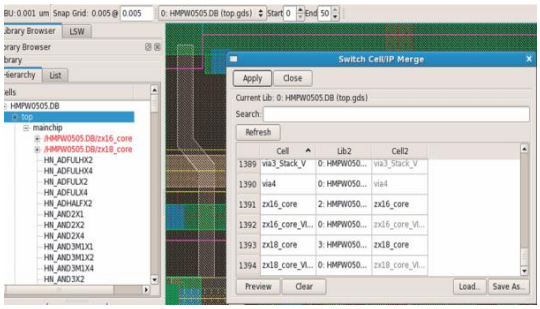

Fig5. Switch Cell/IP Merging

Layout vs Layout(LVL): Skipper allows fast comparison of two large flat or hierarchical layouts in same or different formats. The accuracy is Silicon-proven by thousands of successful tape-out.

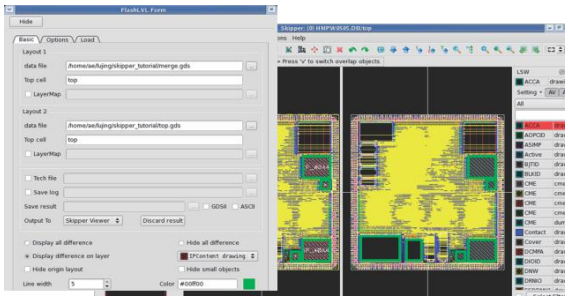

Fig6. Layout Comparison

FIB Data Processing: FIB allows chips to be altered using nano-machining with beams of Gallium ions. Skipper can create layout/edit directives, such as extract area of interest, trace net, cut, connect and probe, for use on the FIB machine to ensure accuracy and reduce turn-round times.

3D Viewing: The 3D viewer can be used for examining layout structures in applications such as FIB and mask data preparation.

Layout watermark: Text information can be added to layout for version record by command or during IP merge process. Watermark can be generated in layout for protecting intellectual property.