Empyrean Argus™

Fast and Accurate DRC/LVS

Benefits

- Cost-effective, in-design DRC/LVS
- Minimal learning curve

Key Features

- High-performance dimensional, density and antenna checking
- User selectable Area-based DRC
- Works with GDSII, OASIS and OpenAccess
- Efficient short-finding
- Integrated debug and analysis environment— Empyrean PVE™

Introduction

Empyrean Argus™ is an accurate and fast physical verification system. Its ***multi-threaded*** architecture offers near-linear scalability in performance (Fig 1) and memory usage. Its ability to process ***commands and data in parallel*** results in delivering consistently high performance. Uses a TCL-based language for rules, which is consistent with industry standard run-sets. With the capability to support any angle layout, Argus is an ideal solution for analog and mixed-signal (big A and small D) designs.

Its built-in graphical and intuitive debug environment enhances user productivity and allows users to debug DRC/LVS output from Empyrean Argus, and as well as other leading third-party DRC tools. Argus supports GDSII, OASIS, and OpenAccess layout formats.

Argus is a ***verification platform***, integrated to Empyrean Aether™ and leading design 3rd party layout editors, enabling full DRC, LVS and integrated debugging. In addition, very fast layout versus layout comparison is made possible by Empyrean FlashLVL™, an integrated companion tool from Argus, multi-threading implementation offers near-linear scaling of performance and memory (Fig 1) utilization. As a result, Argus is very fast on analog and mixed- signal (big A/small D) type of designs.

In additon, Argus allows interactve area based DRC within a user selected window on a given layout. This area-based feature is available as standard from Aether or Skipper® environments when integrated with Argus. The same has been made available to customers from a 3rd party layout environment as a custom capability.

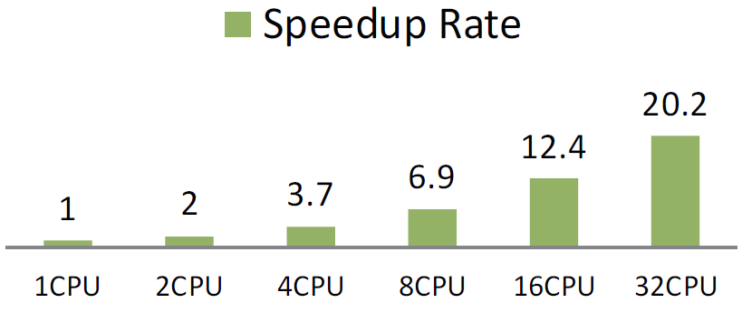

Fig1. Near-linear scalable performance

LVS Features

- Flat and hierarchical LVS
- Netlist vs. netlist analysis
- Electrical rule checks such as path check, sof connect check, etc.
- Intelligent recognition of logic circuits to improve performance and results
- Options to filter dummy devices
- Support for IP-level LVS
- Efficient short finding with LVS-hot-spot (intersection of shorted paths) detection
- Point out schematic differences by semi-logic and semi-database SVS comparison

PVE, the integrated graphical DRC/LVS debug environment, allows easy-to-use analysis and fixing of DRC violations. Fits well as an in-design debug application tool. Using PVE, user can:

- Sort and filter DRC errors and filter duplicate errors
- Read and analyze violation reports from other leading DRC/LVS tools

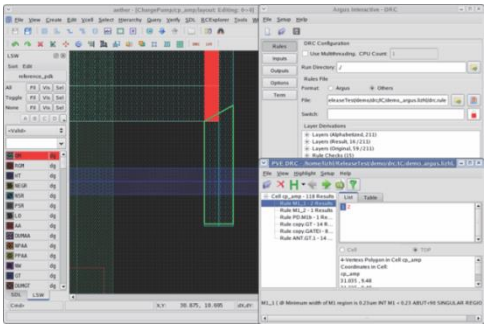

Fig2. Detecting and Fixing DRC Violation

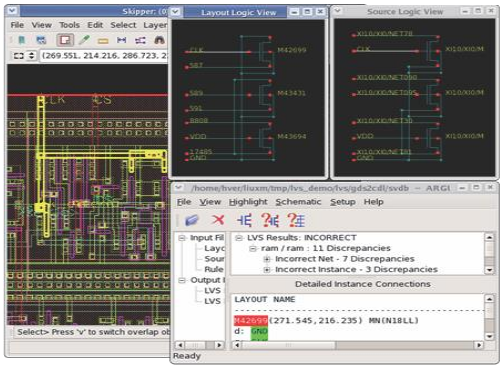

Fig3. LVS Analysis in a Chip Finishing environment using Skipper®

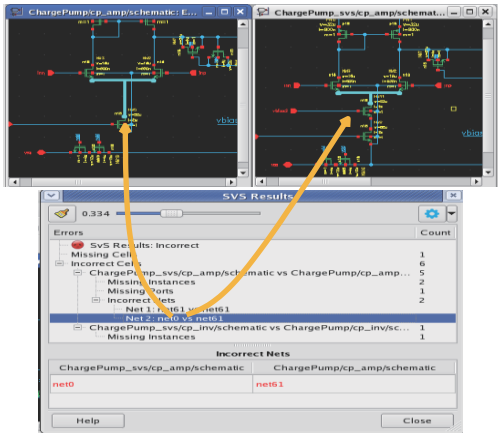

Fig4. SVS Comparison

Supported Platforms

X86 64-bit:

- Red Hat Enterprise V4, V5, and V6

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