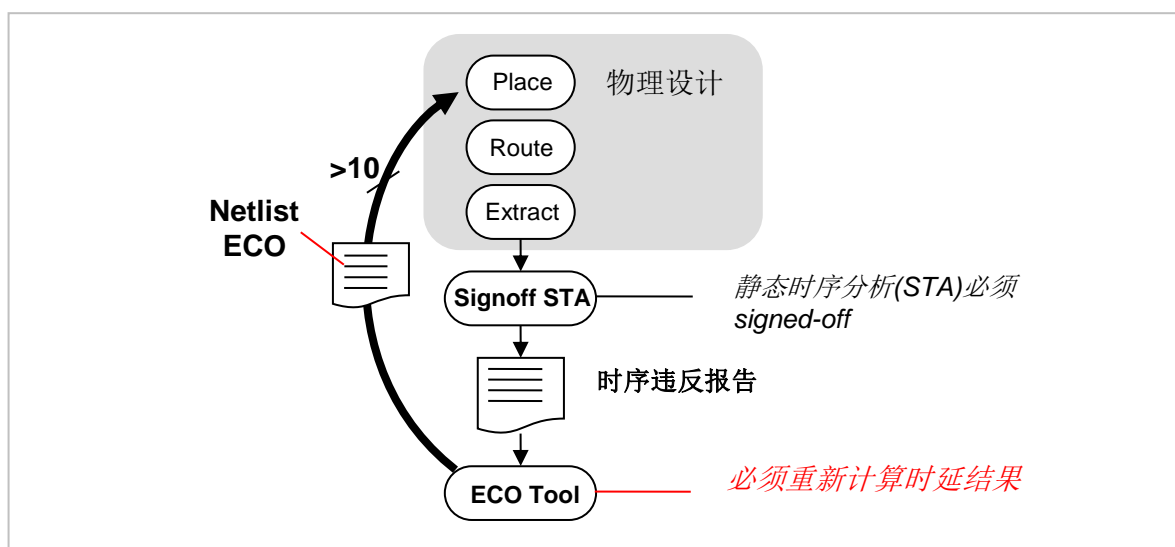


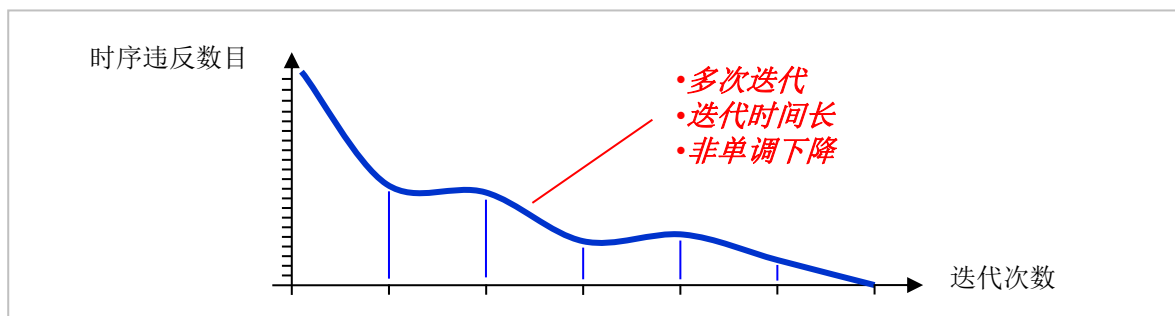
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传统的时序优化 流程

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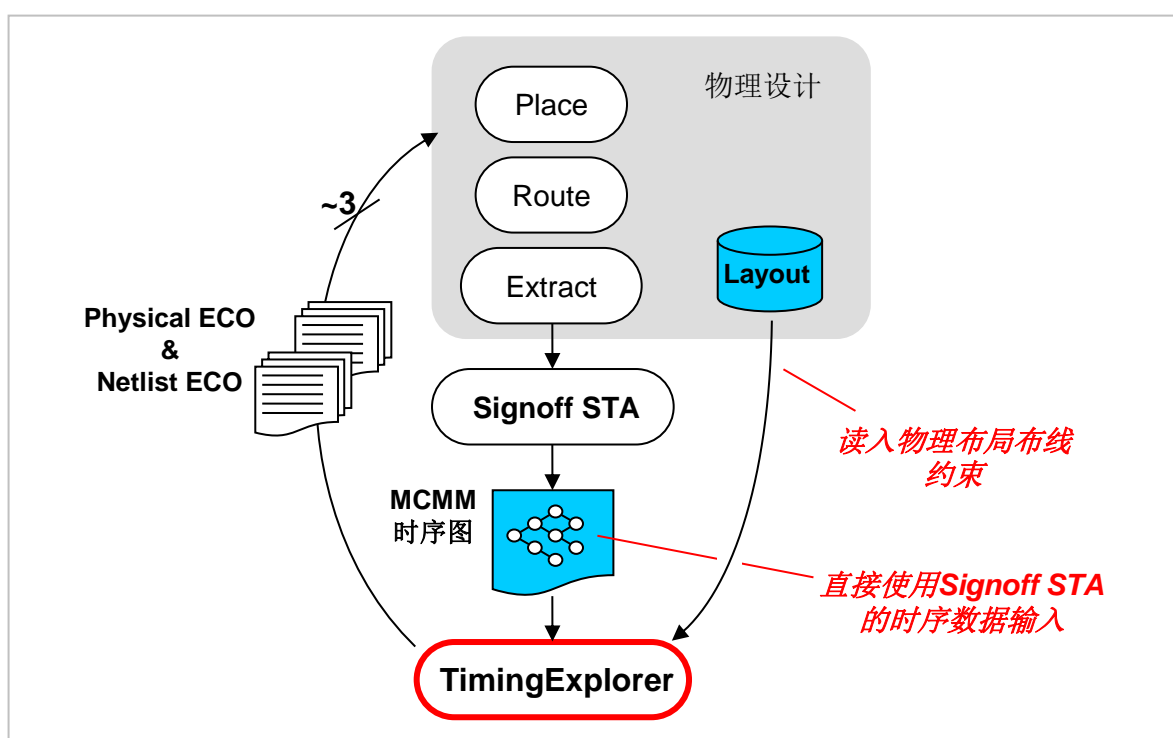
传统 流程的时序违反数目变化

支

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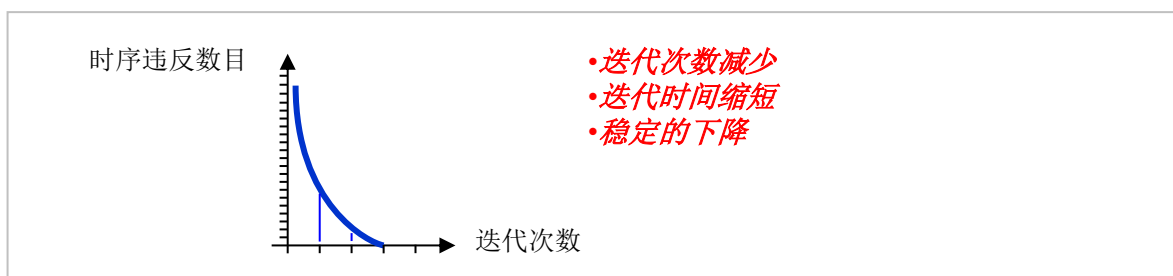
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考虑物理布局布线约束的时序优化 流程

n



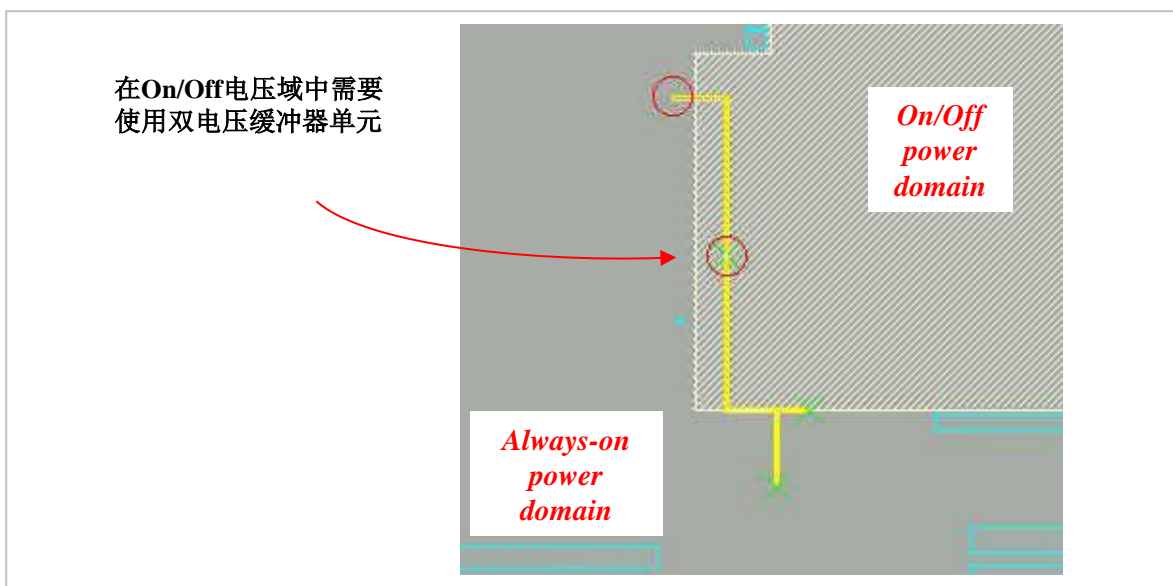
改进的流程可以实现快速时序收敛

支

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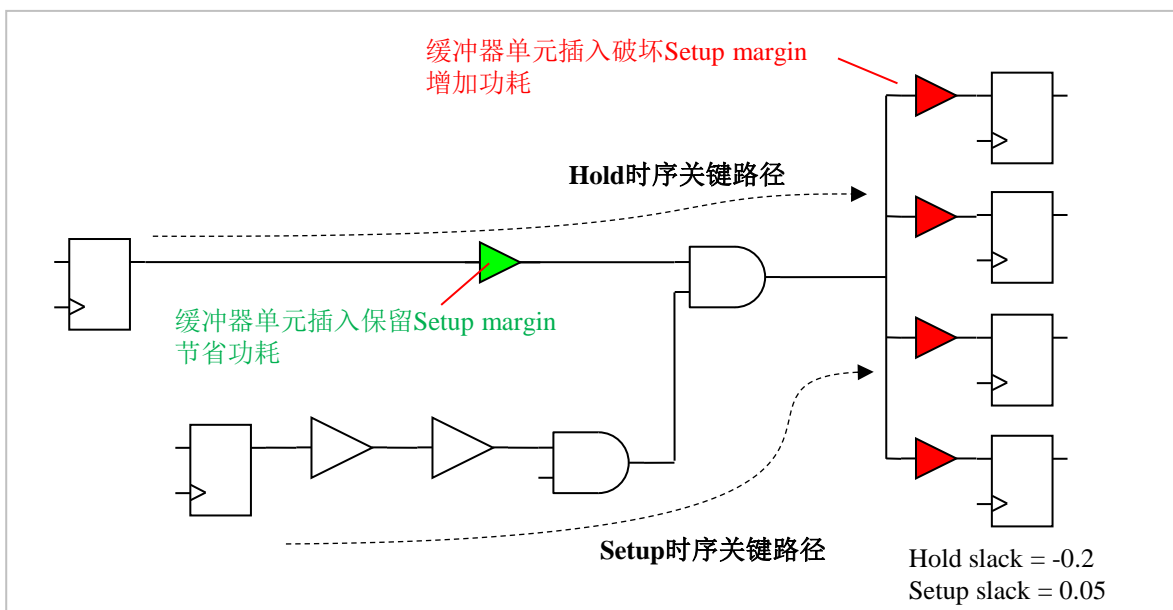


多电压域下单

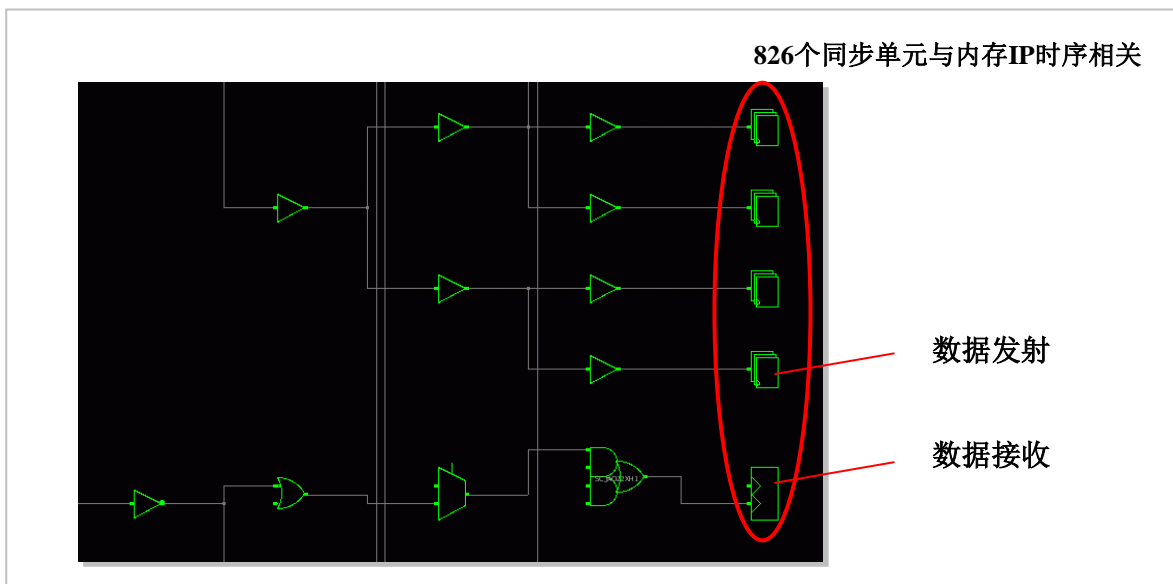
时序修复

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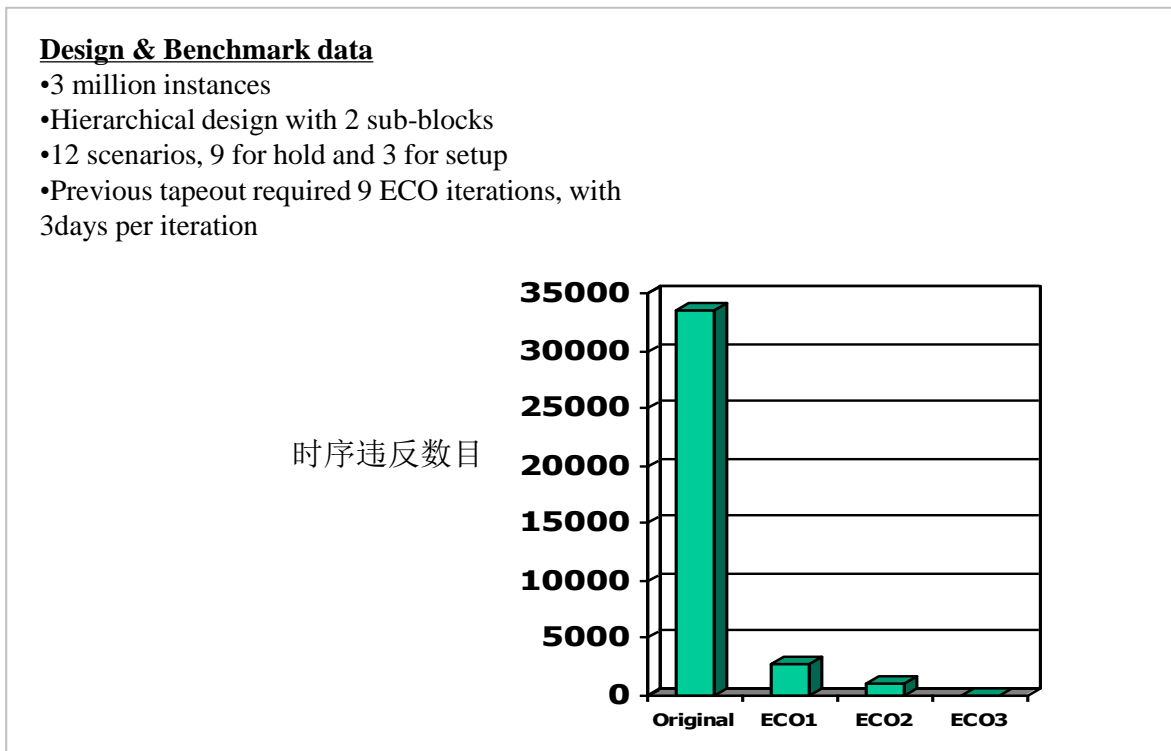
有效的 时序修复：遵循 约束并且节省功耗



时钟偏差影响着时序结果

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的 时序修复结果

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Design & Benchmark data

- 5 million instances total
- 5 scenarios; 12 for hold and 3 for setup

	Run time (HRS)	Buffer count	Setup						Hold					TNS Post
Signoff STA-based ECO														-245
Timing Explorer	3.6	25779	51	51	-0.12	-0.12	-2.3	-2.3	25259	212	-0.82	-0.12	-13476	-21.3

和基于 的 工具的 时序修复对比

Vio# = Number of violations
 Pre = Pre-Optimization
 Post = Post-Optimization
 WNS = Worst Negative Slack
 TNS = Total Negative Slack

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Design & Benchmark data

Process	28 nm
Voltage area count	5
Instance count	4.5M
Gen signoff STA data time	23 min
Design setup time	18 min
Timing fix time	75 min
Total runtime	116 min

	Violations	WNS	TNS	Buffer Count	Dual-rail Buff Count	Gate Sized
Pre-ECO						--
ECO pass1	148	-1.43	-132.6	48217	3342	6216

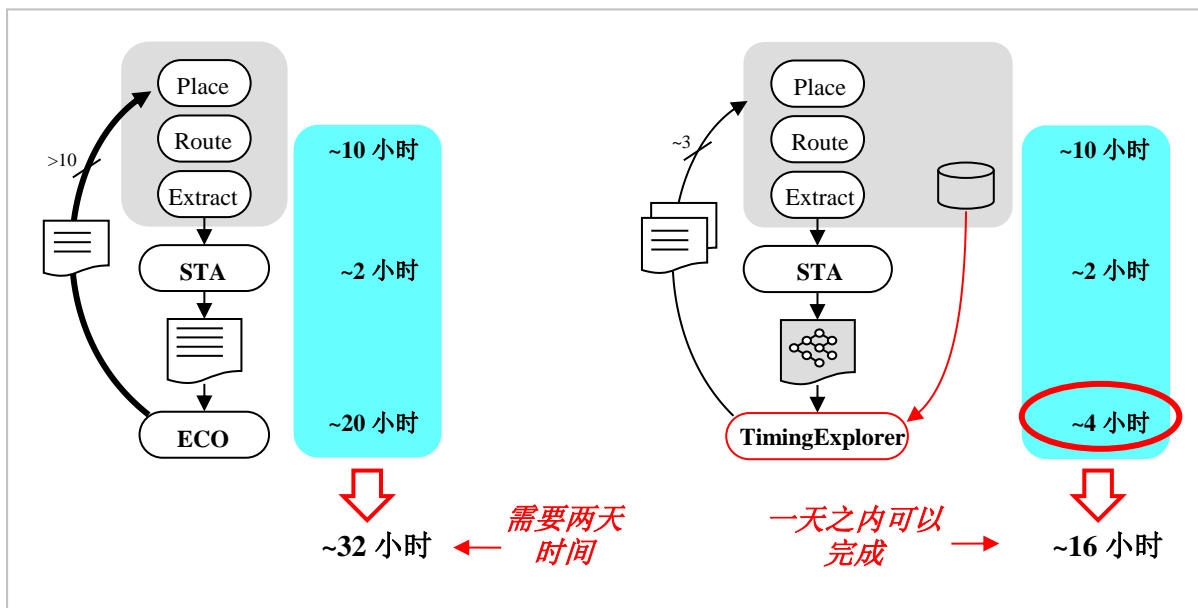
↑ 剩余的时序违反是由于物理布局空间不足所导致

WNS = Worst Negative Slack
TNS = Total Negative Slack

多电压域设计下单

时序修复

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改善的流程大大缩短了迭代时间

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