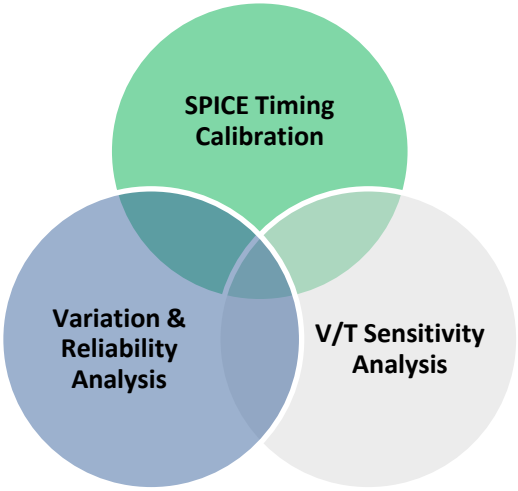
Empyrean XTime™

Statistical SPICE-Accurate Timing Signoff



Overview

Advanced node low power design's pursuit of ultra-low supply voltage is challenging the traditional timing sign-off solution of corner-based static timing analysis. Process effects, like the Miller Effect and the Long Tail Effect, have serious impact on timing performance, resulting in larger discrepancy between the STA calculation data and the actual silicon measurement. For low voltage design, dynamic voltage and frequency scaling (DVFS) scheme, foundries provide a limited number of process corners to model process variation; a new solution is needed to analyze the performance of the design across the entire PVT and RC variation space. Advanced process node's non-Gaussian distribution of process variations are more pronounced at low voltages. While STA tools may incorporate more sophisticated models such as AOCV/POCV/LVF to characterize variation effects, they still incur excessive pessimism or incomplete coverage. Considering variation's effect on reliability, designers need to find a more potent solution.

Empyrean XTime™ provides a SPICE-level fast and accurate timing sign-off solution, to perfectly solve the accuracy problem between STA and silicon for advanced process nodes, 16-nm and beyond, especially for low-voltage IoT design. The built-in V/T sweep function automatically analyzes the sensitivity of timing paths to voltage and temperature variation. Fast Monte-Carlo simulations provide efficient and accurate process variation analysis. The Aging simulation covers dynamic effects to provide a reliability analysis .

XTime has been adopted by a number of chip design companies for timing verification, variable voltage performance prediction, timing signoff criteria formulation, and dynamic effects analysis. The design types include CPU, bitcoin mining, IoT, mobile phone, network, etc. Verified by post-silicon measurement, and silicon's correlation is within ±2%.

Features and Benefits

- **Timing Path Accuracy Signoff**
  - True critical paths validation
  - SPICE calibration for STA timing paths, constraint, and margin
  - Together with XTop™ for SPICE-accurate timing ECO solution
- **Supply Voltage/Temperature Sensitivity Analysis**
  - Voltage sweep for DVFS voltage /frequency tradeoffs prediction
  - IR drop aware SPICE timing paths calibration
  - SPICE simulation based, supply voltage/temperature derating factors characterization
- **Process Variation And Reliability Analysis**
  - Fast Monte Carlo simulation technology enables accurate path-based variation analysis
  - Rapid variation analysis for full coverage of PVT and RC corners

Functionality

❑ SPICE Accuracy Timing Path Verification

❖ Data Calibrated With SPICE Simulation Results

- Slack, frequency
- Launch/capture/data path delay
- Setup/Hold/Pulse width constraint

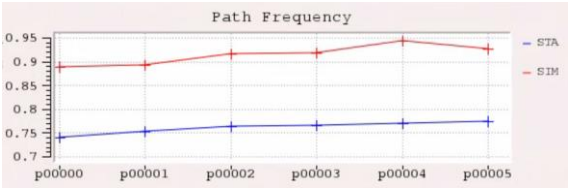


Fig1. STA vs. XTime Comparison

❑ Supply Voltage/Temperature Sensitivity Analysis

❖ Key Features

- Efficient voltage/temperature sweep
- Option to back-annotate IR drop to SPICE simulation
- Big Data Analytics enable critical timing paths verification with voltage/temperature variation

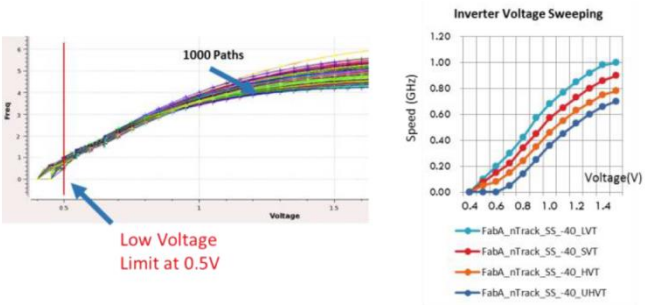


Fig2. Analysis of Low Voltage Limits Based on Voltage Sensitivity

❑ Process Variation/Reliability Analysis

❖ Key Features

- Variation analysis with Fast Monte Carlo simulation
- Reliability analysis of aging effects (e.g. BTI, HCI, …)

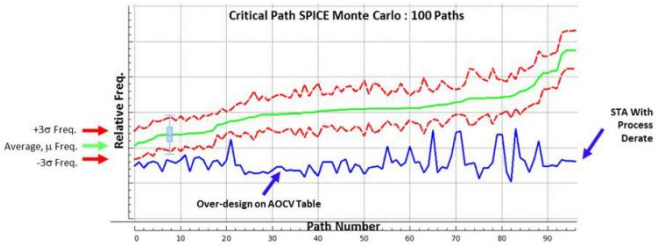


Fig3. Fast Monte Carlo for Process Variation Analysis

Specifications

❑ Input/Output

- Input: Verilog, Liberty, SPEF, LPE SPICE netlist, SPICE model, path report, IR drop file
- Output: SPICE simulation timing data, Timing path report annotated with SPICE timing results

❑ Tool/Flow Integration

- Industry leading EDA design environment
- Command line mode

❑ Supported Platforms

X86 64-bit:

- Red Hat Enterprise V4, V5, and V6

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