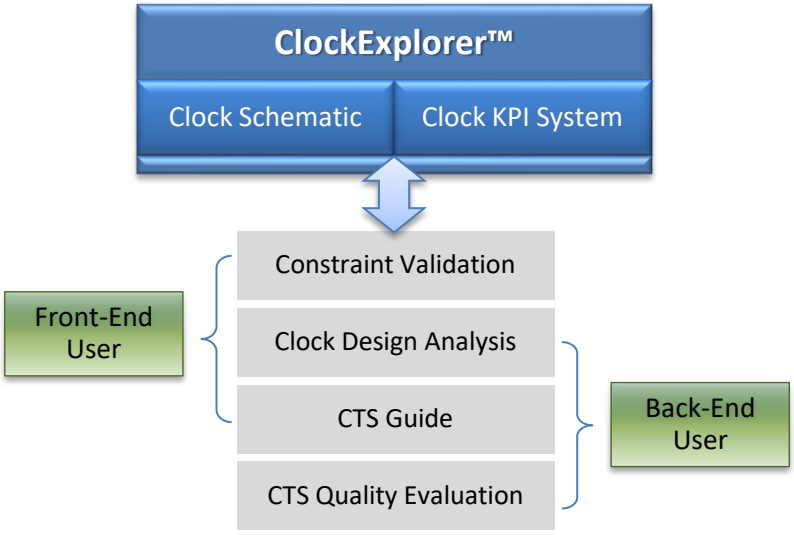
ClockExplorer™

Rule-Based Diagnosis for Superior Clock



Overview

As technology nodes move into 16nm and below, the SoC design scale and complexity increase rapidly. The impact of the clock network on the quality of entire design increases. Problems on the clock can lead to project delay, chip revision, and loss of yield. Therefore, the potential risks of clock need to be considered as early as possible in the design process.

For front/middle-end engineers, before signoff RTL codes sdc files, they need to avoid the unfriendly structure and inappropriate constraints. For back-end engineers, in order to reduce CTS design cycle, they need to optimize CTS strategies by checking physical placement of clock network and analyzing clock structure. For the undesired CTS results, the bottleneck identification and modification need to be done before a new iteration. All these requires designers lots of efforts and years of experiences.

ClockExplorer™, a dedicated clock analysis and diagnosis platform, is developed to solve the clock design difficulties in each stage, reduce the clock design cycle and get better CTS results. It has the most powerful clock schematic viewer to help designers sort out clock tree structures and develop better CTS strategies. The embedded comprehensive clock check within a KPI (Key Performance Indicator) system helps designers evaluate the clock design quality, find out the bottlenecks and improve the CTS quality.

ClockExplorer has been adopted and proven its high value in world-leading IC design companies. Its clock schematic is considered as the clearest and the most concise clock structure viewer by almost all users. The clock KPI system has been used for scoring the clock design quality of each stage in top 20 design houses and plays a key role in their clock design flow.

Features and Benefits

- **Powerful Clock Schematic**
  - Concise clock structure viewer
  - Complex clock and group relationship clarification
  - Better CTS strategy for higher clock synthesis quality
  - Interactive connection tracing & real time physical cross probing
- **Rule-based Clock KPI System**
  - One-click clock quality evaluation for pre-CTS & post-CTS clock design quality checking
  - Easy to know bottleneck of CTS result analysis & improvement
  - Timing dependency analysis connecting the clock & timing
  - Reduced clock design cycle, lower clock power and OCV

Functionality

❑ Powerful Clock Schematic

❖ Advanced Schematic Mode

- Overview mode with advanced modulization
- Viewing by_delay and by_level mode
- Group schematic with multiple clocks in one schematic

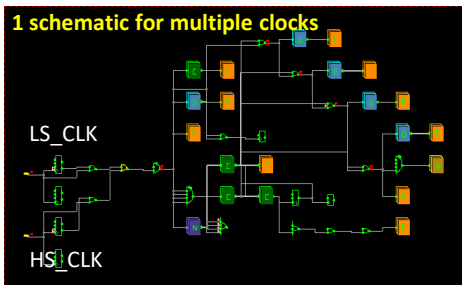


Fig1. Clock Group Schematic

❖ Useful Analysis & Debugging

- Cone schematic to trace cell/pin connection
- Cross probing with layout viewer
- Flyline to show timing dependent connection

❑ Rule-based Clock KPI System

❖ One-click Clock Quality Evaluation

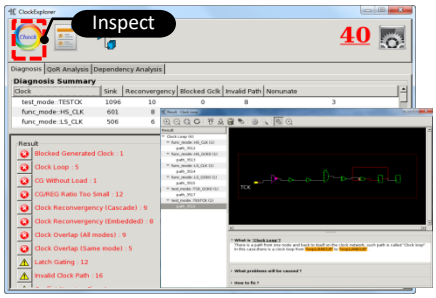


Fig2. Clock KPI Main Window

❖ Quality Checking

- Clock diagnosis

  Sdc validation, unfriendly structure detection, …
- Clock QoR analysis

  Physical bottleneck detection, DRC checking, …
- Timing dependency check

  Advanced cell/net skew analysis, early branch analysis, …

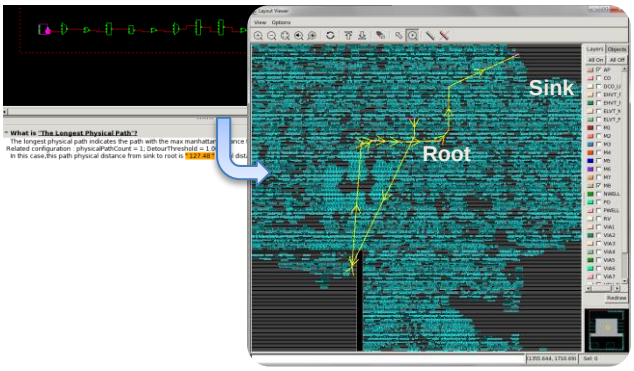


Fig3. QoR Analysis: finding out the longest physical path which causes more CTS buffers and longer latency

Specifications

❑ Input Files

- LEF, timing library, Verilog, DEF, sdc, clock spec, sdf

❑ Flow Integration

- Industry leading EDA design environment
- Standalone Tcl command line

❑ System Supported

X86 64-bit:

- Red Hat Enterprise V4, V5, and V6

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